
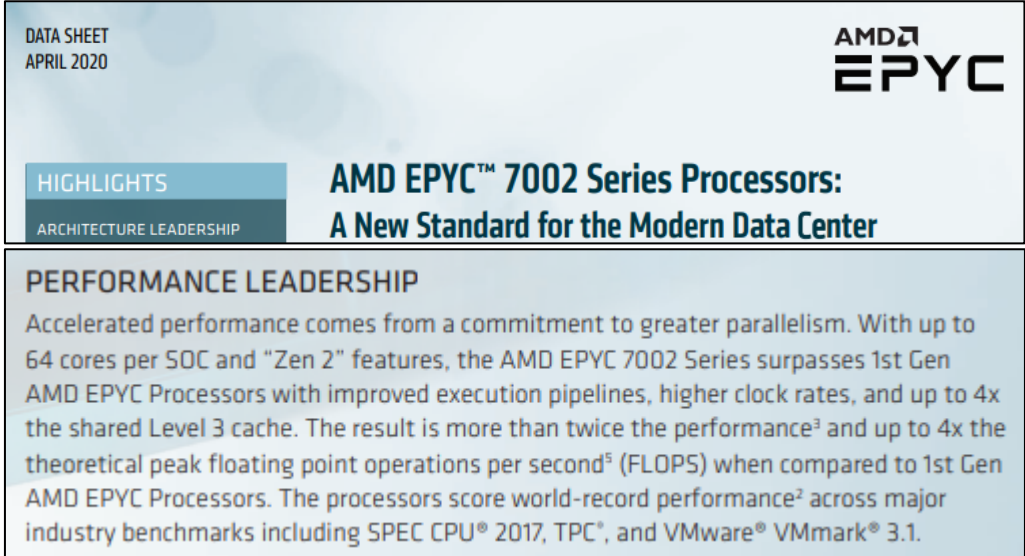
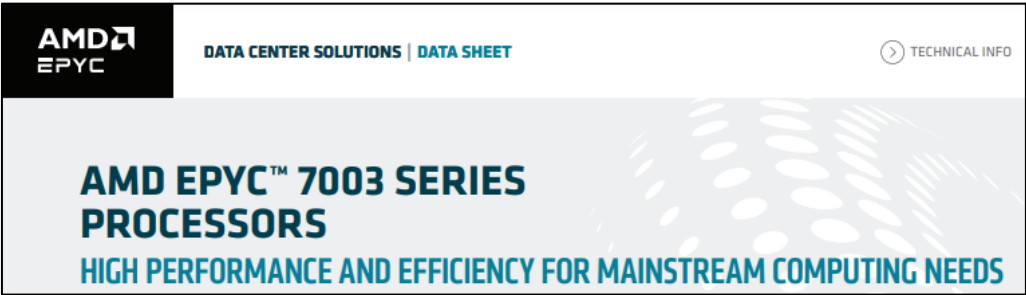


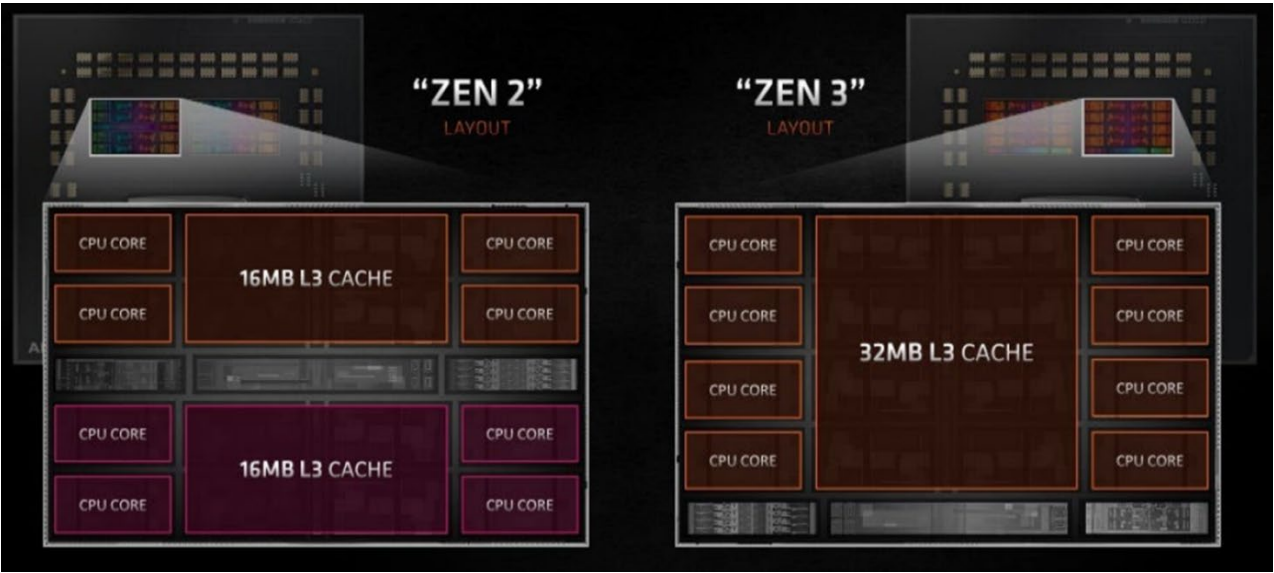
EXHIBIT 14

Exhibit 14: U.S. Patent No. 6,871,264

Claim 1	Identification
<p>1[pre]. A processor integrated circuit capable of executing more than one instruction stream comprising:</p>	<p>To the extent the preamble is limiting, SAP provides a processor integrated circuit capable of executing more than one instruction stream. For example, <i>see</i>:</p>  <p>Source: https://www.youtube.com/watch?v=ECHhuvuiNzs (Nov. 8, 2021)</p>

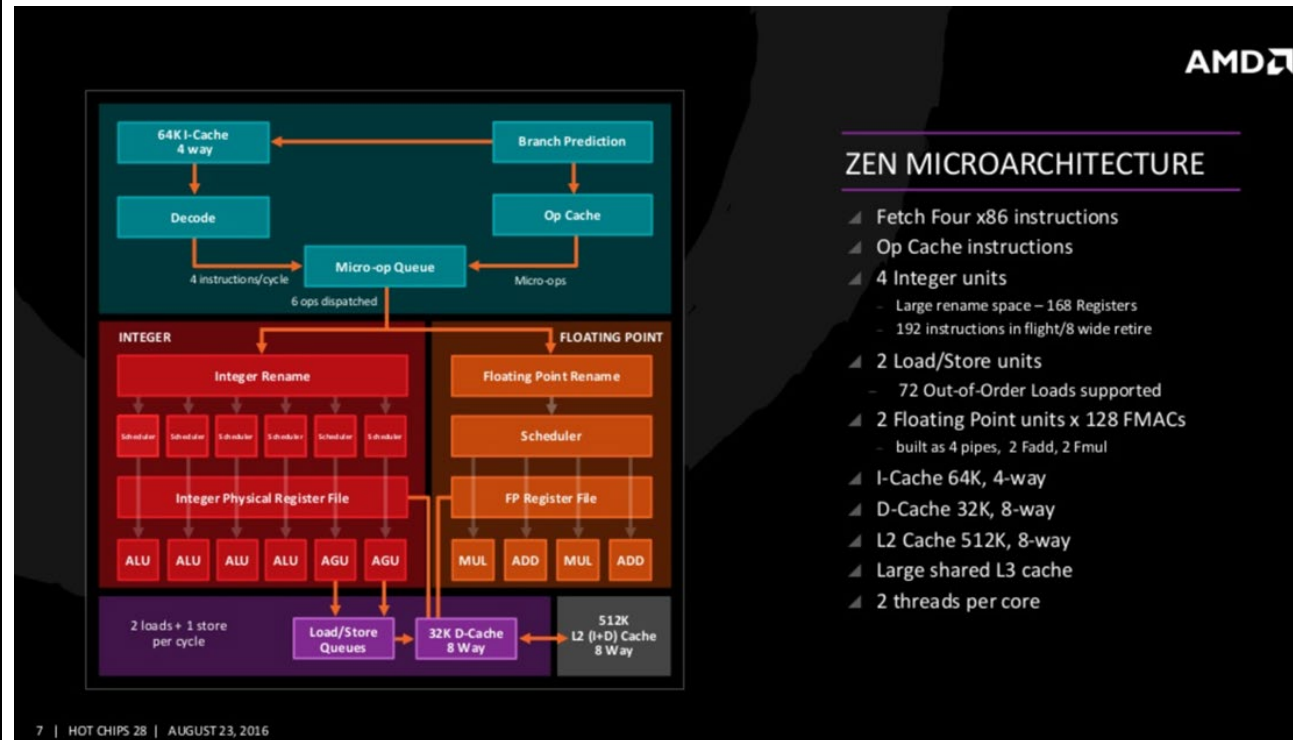
Claim 1	Identification
	<div data-bbox="590 269 1524 321" style="border: 1px solid black; padding: 5px;"> AMD EPYC CPUs Now Power SAP Applications Hosted on Google Cloud </div> <div data-bbox="590 329 1524 594" style="border: 1px solid black; padding: 5px;"> <p>SANTA CLARA, Calif., July 11, 2023 (GLOBE NEWSWIRE) -- Today, AMD (NASDAQ: AMD) announced that SAP has chosen AMD EPYC™ processor-powered Google Cloud N2D virtual machines (VMs) to run its cloud ERP delivery operations for RISE with SAP; further increasing adoption of AMD EPYC for cloud-based workloads. As enterprises look toward digital modernization, many are adopting cloud-first architectures to complement their on-premises data centers. AMD, Google Cloud and SAP can help customers achieve their most stringent performance goals while delivering on energy efficiency, scalability and resource utilization needs.</p> </div> <div data-bbox="590 602 1524 781" style="border: 1px solid black; padding: 5px;"> <p>"As part of our RISE with SAP initiative, we have made a strategic decision to add AMD EPYC processor powered N2D instances in Google Cloud to run mission critical workloads for our enterprise cloud customers." said Lalit Patil, CTO, SAP Enterprise Cloud Services, SAP SE. "Our engineering collaboration with AMD and Google Cloud can result in an increase in performance and performance-per-dollar over comparable instances."</p> </div> <div data-bbox="583 789 1854 857" style="border: 1px solid black; padding: 5px;"> <p>Source: https://www.amd.com/en/newsroom/press-releases/2023-7-11-amd-epyc-cpus-now-power-sap-applications-hosted-on.html</p> </div> <div data-bbox="590 898 1692 1146" style="border: 1px solid black; padding: 5px;"> <p>— What is the difference between SAP S/4HANA Cloud, private edition and RISE with SAP?</p> <p>SAP S/4HANA Cloud, private edition is the cloud ERP at the heart of RISE with SAP. RISE with SAP bundles software that includes the cloud ERP, process intelligence and execution, advanced office of the CFO features, and more, along with a complete cloud infrastructure and migration services.</p> </div> <div data-bbox="583 1154 1331 1187" style="border: 1px solid black; padding: 5px;"> <p>Source: https://www.sap.com/africa/products/erp/rise.html</p> </div>

Claim 1	Identification
	<div data-bbox="583 269 1602 821">  <p>DATA SHEET APRIL 2020</p> <p>AMD EPYC</p> <p>HIGHLIGHTS ARCHITECTURE LEADERSHIP</p> <p>AMD EPYC™ 7002 Series Processors: A New Standard for the Modern Data Center</p> <p>PERFORMANCE LEADERSHIP</p> <p>Accelerated performance comes from a commitment to greater parallelism. With up to 64 cores per SOC and “Zen 2” features, the AMD EPYC 7002 Series surpasses 1st Gen AMD EPYC Processors with improved execution pipelines, higher clock rates, and up to 4x the shared Level 3 cache. The result is more than twice the performance³ and up to 4x the theoretical peak floating point operations per second⁵ (FLOPS) when compared to 1st Gen AMD EPYC Processors. The processors score world-record performance² across major industry benchmarks including SPEC CPU® 2017, TPC®, and VMware® VMmark® 3.1.</p> </div> <p>Source: https://www.amd.com/system/files/documents/AMD-EPYC-7002-Series-Datasheet.pdf; see also https://www.amd.com/en/processors/epyc-7002-series.</p> <div data-bbox="730 938 1749 1230">  <p>AMD EPYC</p> <p>DATA CENTER SOLUTIONS DATA SHEET</p> <p>TECHNICAL INFO</p> <p>AMD EPYC™ 7003 SERIES PROCESSORS</p> <p>HIGH PERFORMANCE AND EFFICIENCY FOR MAINSTREAM COMPUTING NEEDS</p> </div> <div data-bbox="625 1235 1850 1349"> <p>Workhorse data center portfolio: AMD EPYC 7003 Series processors have set a standard for performance and efficiency for a generation of mainstream servers with the combination of powerful ‘Zen 3’ cores, scalability from 8 to 64 cores per processors, up to 8 channels of fast, inexpensive DDR4 memory and up to 128 lanes of high-throughput PCIe Gen 4 I/O. With strong performance across the portfolio and attractive pricing, you can cost-effectively extend the value of your IT infrastructure investment by choosing 3rd Gen AMD EPYC processors.</p> </div>

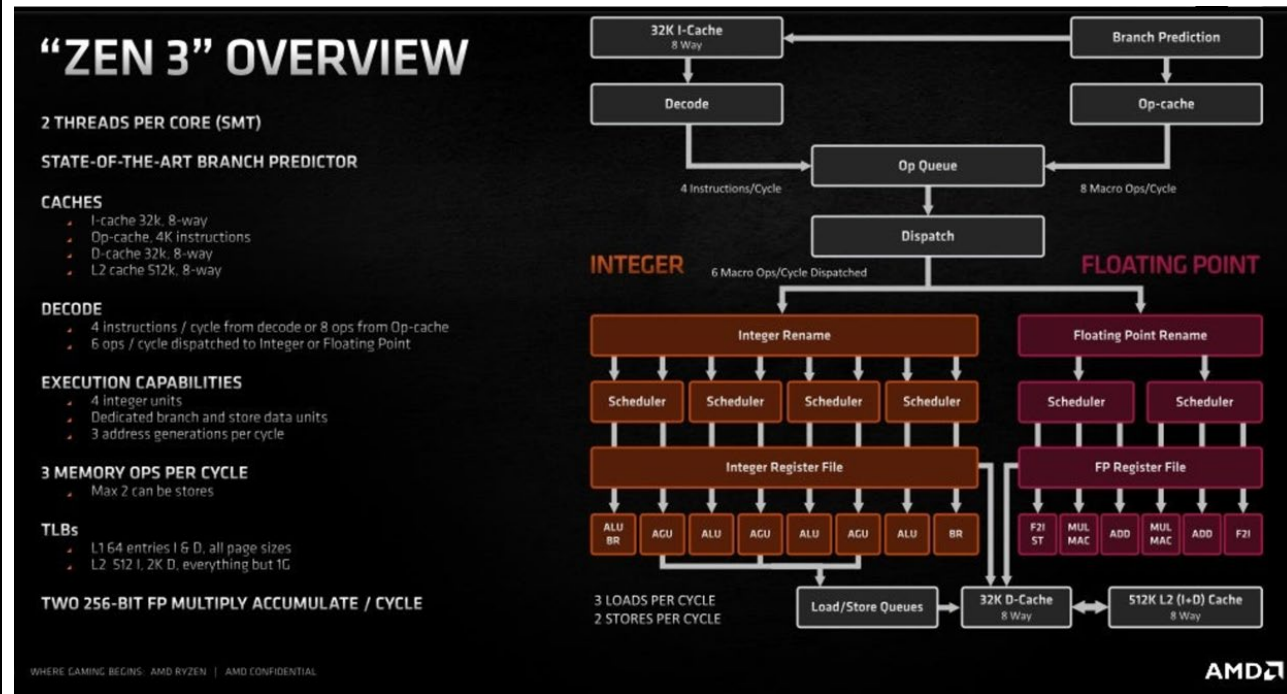
Claim 1	Identification
	<p data-bbox="583 235 1871 305">Source: https://www.amd.com/system/files/documents/amd-epyc-7003-series-datasheet.pdf; <i>see also</i> https://www.amd.com/en/processors/epyc-7003-series.</p>  <p data-bbox="583 911 1772 1015">Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; <i>see also</i> https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.</p>

Claim 1

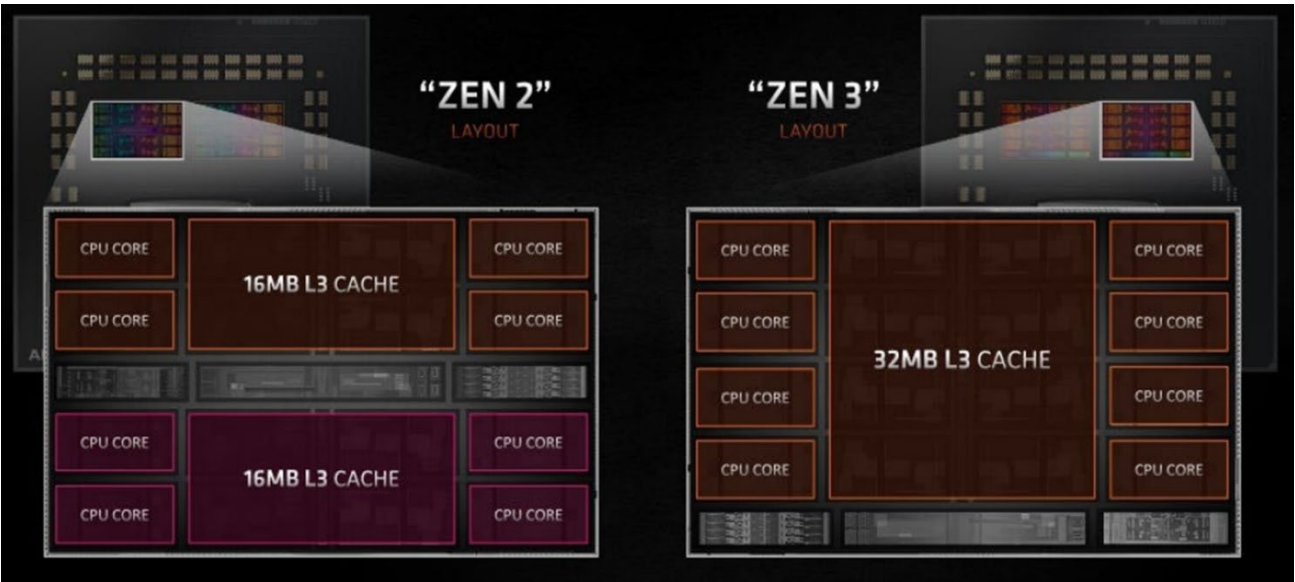
Identification



Source: <https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html>; see <https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core>; <https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28>.

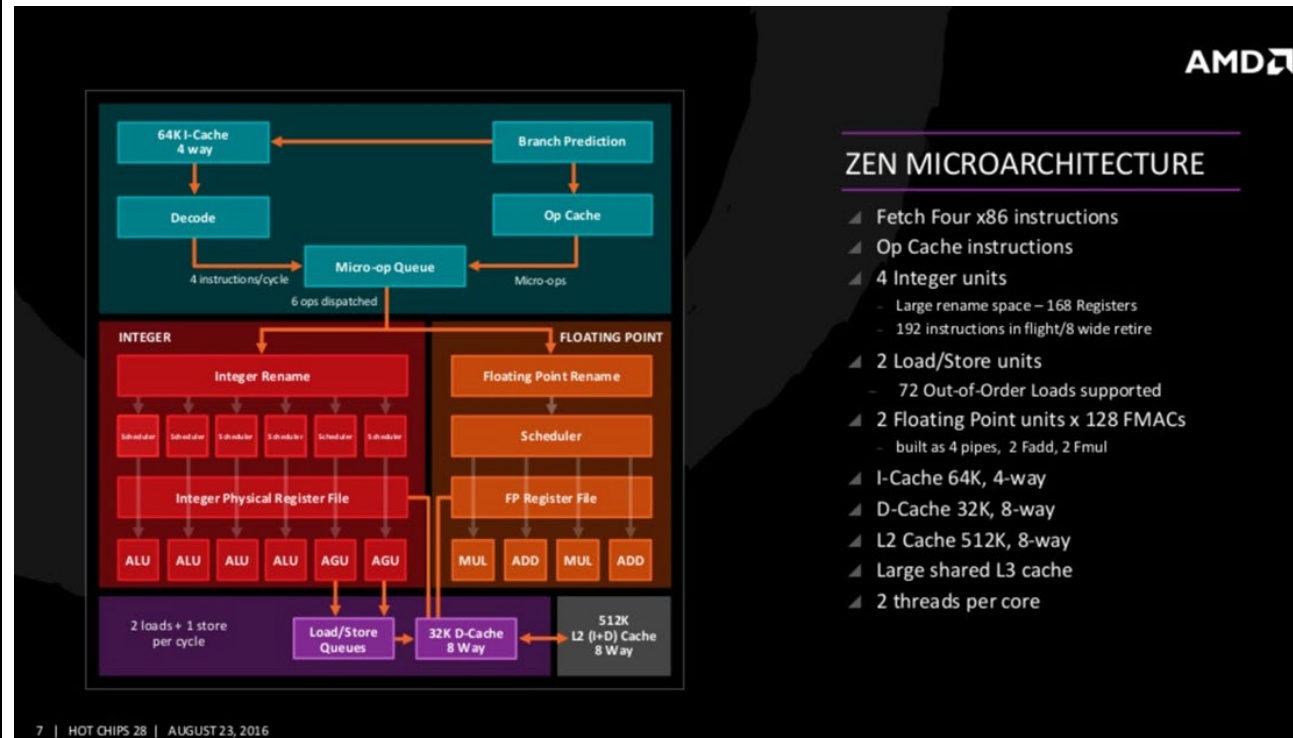
Claim 1**Identification**

Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; see also <https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3>.

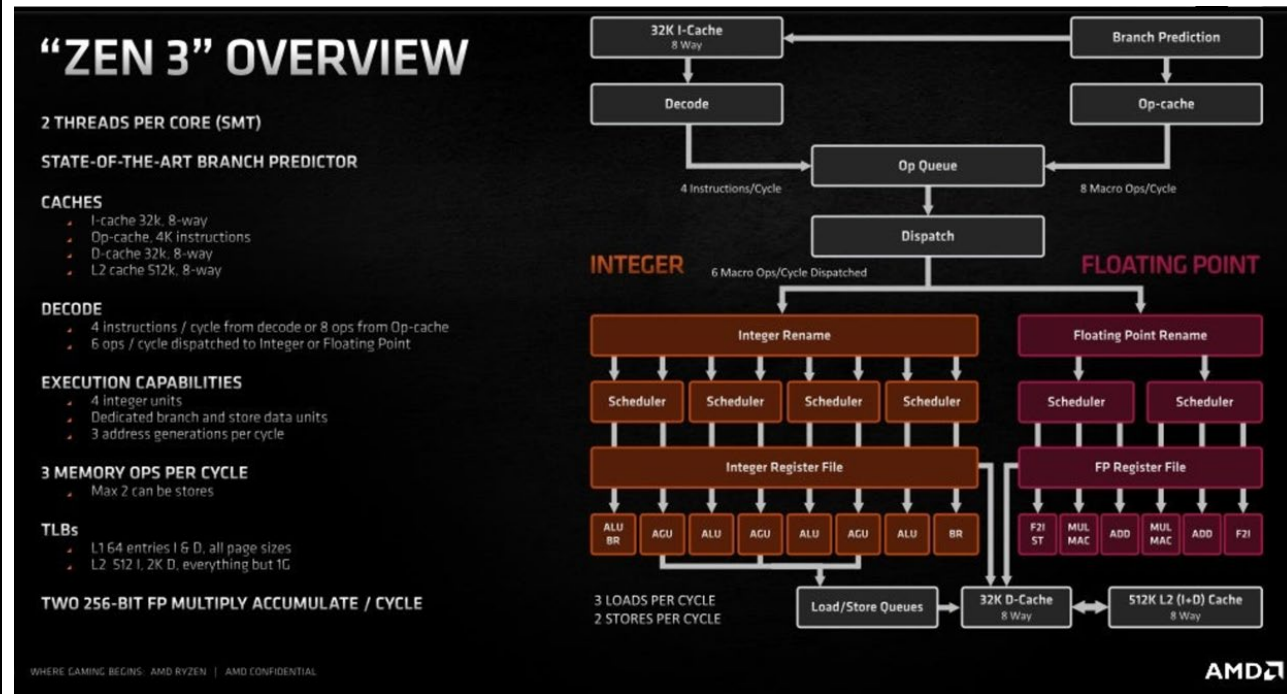
Claim 1	Identification
<p>1[a]. a first processor, coupled to fetch instructions and access data through a first cache controller;</p>	<p>SAP provides a first processor, coupled to fetch instructions and access data through a first cache controller. For example, <i>see</i>:</p>  <p>Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; <i>see also</i> https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.</p>

Claim 1

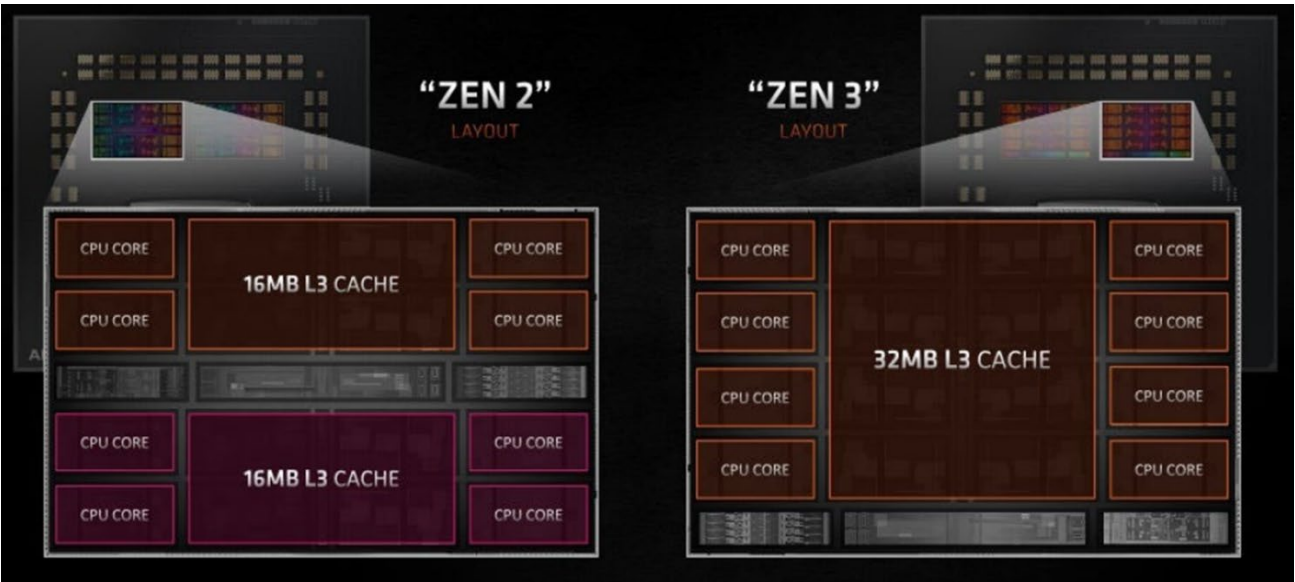
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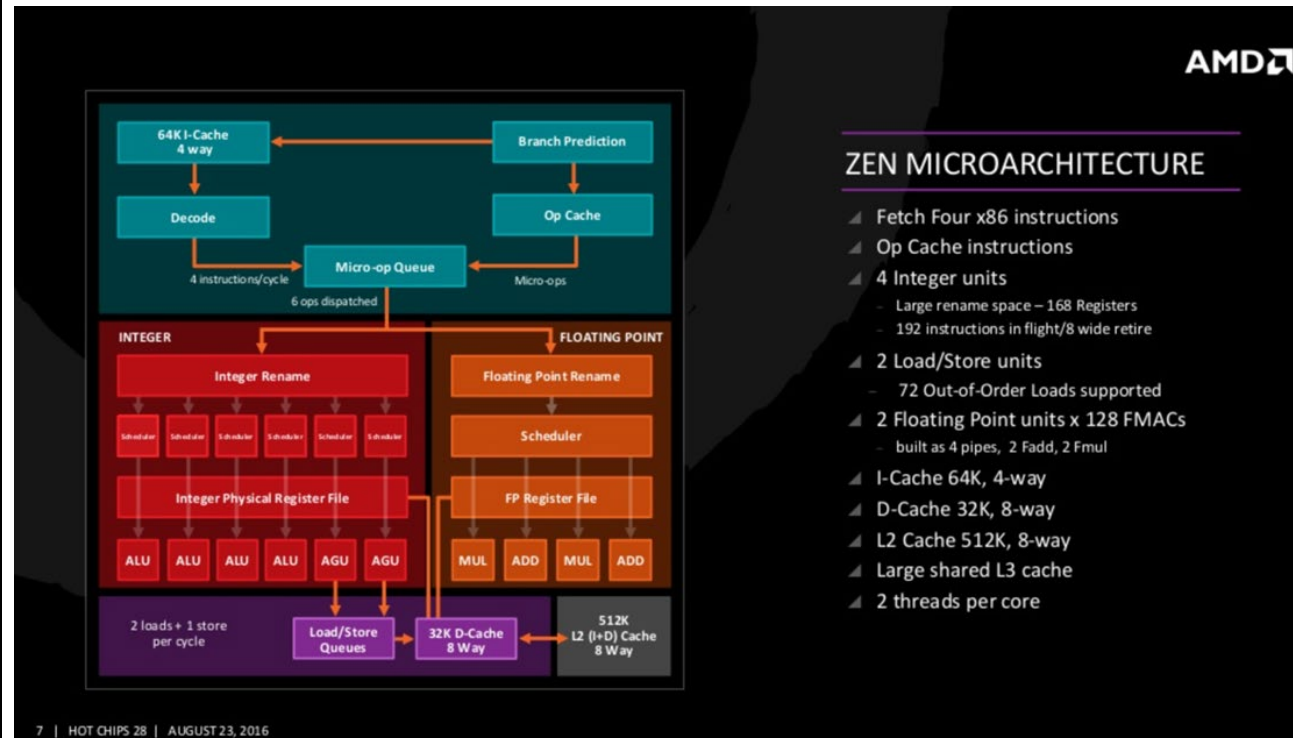


Source: <https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html>; see <https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core>; <https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28>.

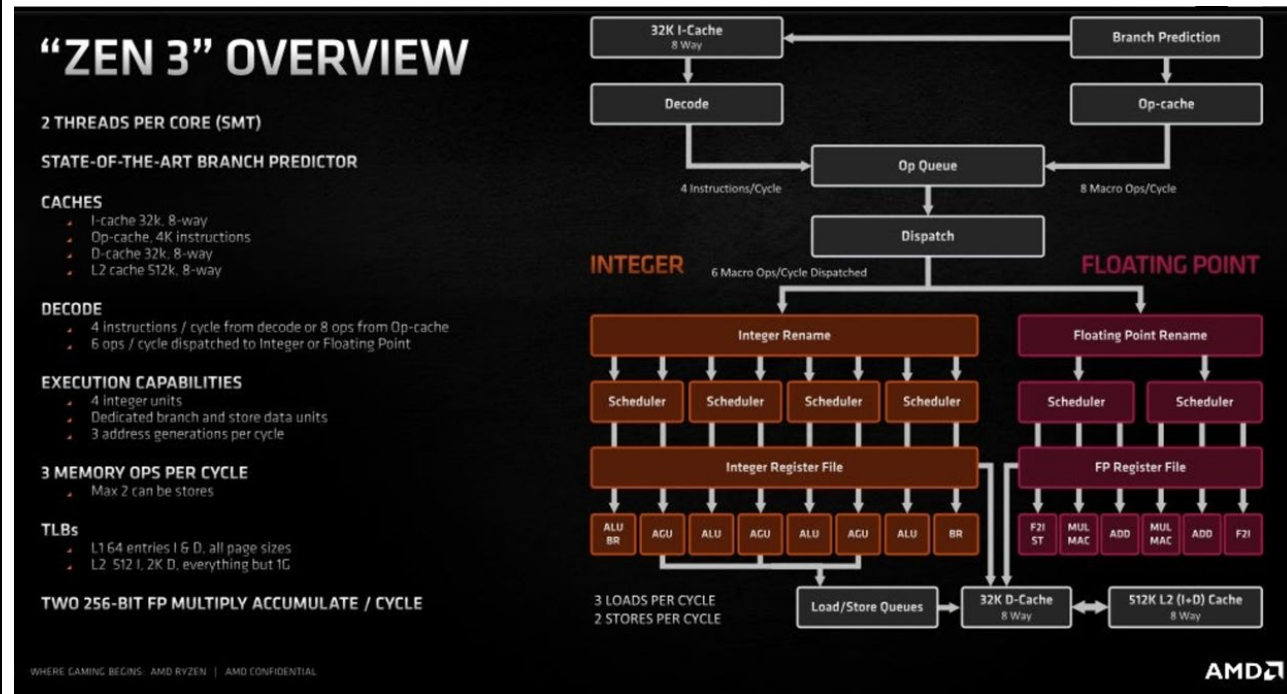
Claim 1**Identification**

Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; see also <https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3>.


Claim 1	Identification
<p>1[b]. a second processor, coupled to fetch instructions and access data through a second cache controller;</p>	<p>SAP provides a second processor, coupled to fetch instructions and access data through a second cache controller. For example, <i>see</i>:</p>  <p>Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; <i>see also</i> https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.</p>

Claim 1**Identification**

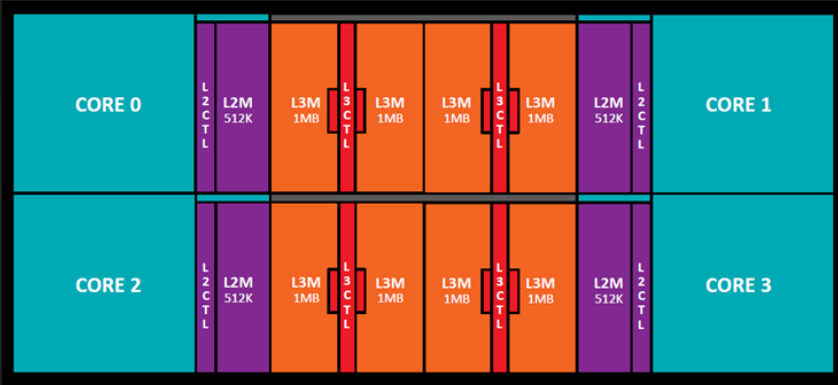
Source: <https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html>; see <https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core>; <https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28>.

Claim 1**Identification**

Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; see also <https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3>.

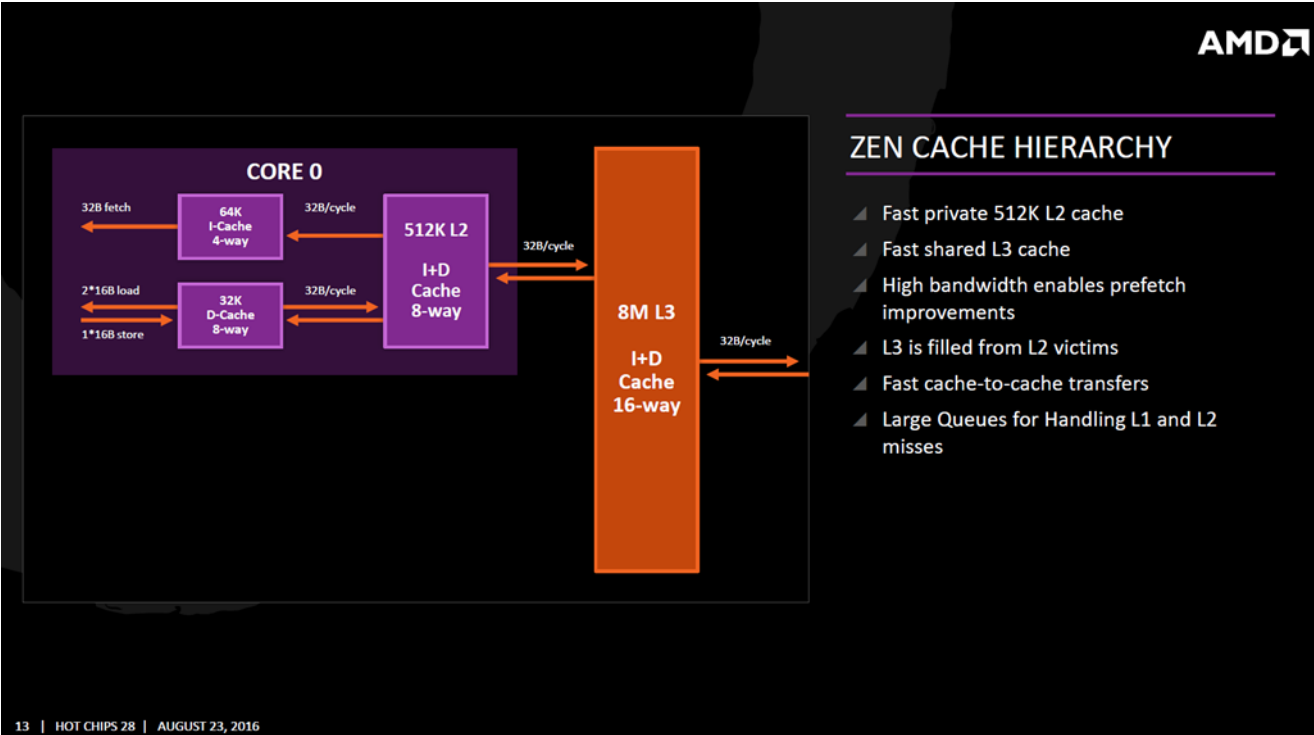
Claim 1	Identification
<p>1[c]. a plurality of cache memory blocks;</p>	<p>SAP provides a plurality of cache memory blocks. For example, <i>see</i>:</p>  <p>The diagram illustrates the internal architecture of two AMD processors: ZEN 2 and ZEN 3. On the left, the ZEN 2 layout is shown with two identical processing units. Each unit consists of a central 16MB L3 cache block (highlighted in purple) flanked by four CPU cores (orange boxes). On the right, the ZEN 3 layout is shown with a single processing unit featuring a larger central 32MB L3 cache block (highlighted in orange) flanked by eight CPU cores (orange boxes). The background of each layout shows a detailed view of the processor die with various functional blocks.</p> <p>Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; <i>see also</i> https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.</p>

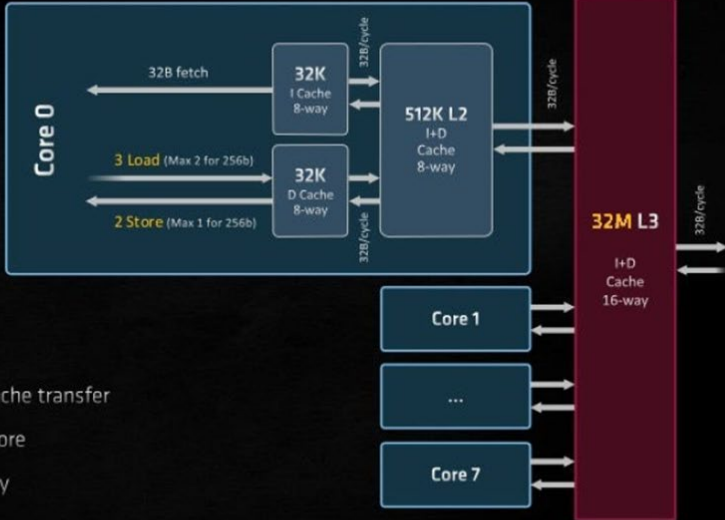
Claim 1	Identification
	<div data-bbox="577 264 1890 995"> <p>ZEN CACHE HIERARCHY</p> <ul style="list-style-type: none"> Fast private 512K L2 cache Fast shared L3 cache High bandwidth enables prefetch improvements L3 is filled from L2 victims Fast cache-to-cache transfers Large Queues for Handling L1 and L2 misses <p>13 HOT CHIPS 28 AUGUST 23, 2016</p> </div> <p>Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; see https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.</p>

Claim 1	Identification
	<div data-bbox="583 264 1871 987">  <p>The diagram illustrates the AMD Zen CPU Complex architecture. It shows four cores (CORE 0, CORE 1, CORE 2, CORE 3) arranged in a 2x2 grid. Each core is connected to a shared L3 cache. The L3 cache is composed of four slices, each 1MB in size, connected to a central L3 cache controller (L3 CTL). Each core also has its own L2 cache (L2M, 512K) and a local L2 cache controller (L2 CTL). The L3 cache is 16-way associative and 8MB in size, mostly exclusive of L2. The L3 cache is made of 4 slices, by low-order address interleave. Every core can access every cache with same average latency.</p> <p>CPU COMPLEX</p> <ul style="list-style-type: none"> ▲ A CPU complex (CCX) is four cores connected to an L3 Cache. ▲ The L3 Cache is 16-way associative, 8MB, mostly exclusive of L2. ▲ The L3 Cache is made of 4 slices, by low-order address interleave. ▲ Every core can access every cache with same average latency <p>14 HOT CHIPS 28 AUGUST 23, 2016</p> </div> <p>Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; see https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.</p>

Claim 1	Identification
	<div data-bbox="583 261 1892 963"> <h2 style="margin: 0;">“ZEN 3” CACHE HIERARCHY (8-CORE)</h2> <ul style="list-style-type: none"> ➤ Fast private 512K L2 cache ➤ High bandwidth enables prefetch improvements ➤ L3 is filled from L2 victims (i.e. mostly exclusive) ➤ L2 tags duplicated in L3 for probe filtering and fast cache transfer ➤ 64 outstanding misses supported from L2 to L3 per core ➤ 192 outstanding misses supported from L3 to memory ➤ L3 shared among all 8 cores in the complex <p style="font-size: small; margin-top: 10px;">20 WHERE GAMING BEGINS. AMD RYZEN AMD CONFIDENTIAL</p> </div> <p style="margin-top: 10px;">Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; see also https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.</p>

Claim 1	Identification												
	<div><div><div><div>63</div><div>Reserved, MBZ</div><div>CBM_LEN</div><div>0</div><div>MASK</div></div><div>L3_MASK_n, MSR C90h + n</div><div>...</div><div><div><div>63</div><div>Reserved, MBZ</div><div>CBM_LEN</div><div>0</div><div>MASK</div></div><div>L3_MASK_1, MSR C91h</div><div><div><div>63</div><div>Reserved, MBZ</div><div>CBM_LEN</div><div>0</div><div>MASK</div></div><div>L3_MASK_0, MSR C90h</div></div><table><thead><tr><th>Bits</th><th>Mnemonic</th><th>Description</th><th>R/W</th></tr></thead><tbody><tr><td>63:CBM_LEN+1</td><td>Reserved</td><td>Reserved, MBZ</td><td></td></tr><tr><td>CBM_LEN:0</td><td>MASK</td><td>L3 Cache PQE Allocation Mask</td><td>R/W</td></tr></tbody></table><div>L3_MASK_<COS> MSR Registers</div></div></div><div>Source: https://web.archive.org/web/20210305161038/https://developer.amd.com/wp-content/resources/56375_1.00.pdf</div></div>	Bits	Mnemonic	Description	R/W	63:CBM_LEN+1	Reserved	Reserved, MBZ		CBM_LEN:0	MASK	L3 Cache PQE Allocation Mask	R/W
Bits	Mnemonic	Description	R/W										
63:CBM_LEN+1	Reserved	Reserved, MBZ											
CBM_LEN:0	MASK	L3 Cache PQE Allocation Mask	R/W										

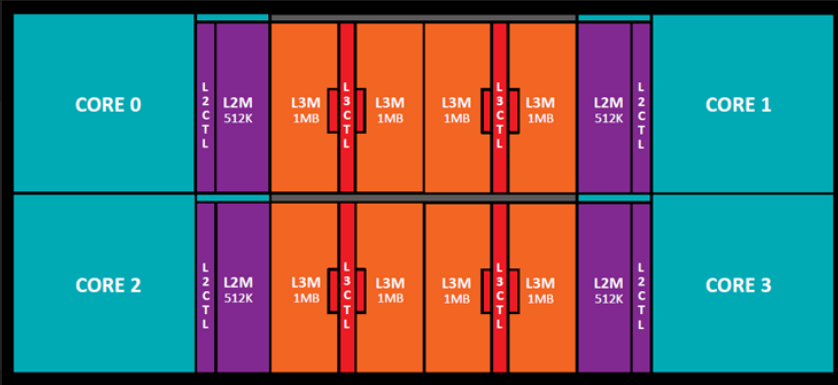
Claim 1	Identification
<p>1[d]. a high-speed interconnect coupling the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers;</p> <p>and</p>	<p>SAP provides a high-speed interconnect coupling the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers. For example, <i>see</i>:</p>  <p>Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; <i>see</i> https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.</p>

Claim 1	Identification
	<div data-bbox="583 264 1892 963"> <h2 style="margin: 0;">“ZEN 3” CACHE HIERARCHY (8-CORE)</h2> <ul style="list-style-type: none"> ➤ Fast private 512K L2 cache ➤ High bandwidth enables prefetch improvements ➤ L3 is filled from L2 victims (i.e. mostly exclusive) ➤ L2 tags duplicated in L3 for probe filtering and fast cache transfer ➤ 64 outstanding misses supported from L2 to L3 per core ➤ 192 outstanding misses supported from L3 to memory ➤ L3 shared among all 8 cores in the complex  <p style="font-size: small; margin-top: 10px;">20 WHERE GAMING BEGINS. AMD RYZEN AMD CONFIDENTIAL</p> </div> <p style="margin-top: 10px;">Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; see also https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.</p>

Claim 1	Identification
	<p data-bbox="632 282 905 318">QOS Enforcement</p> <p data-bbox="632 334 1619 509">QOS enforcement is accomplished by assigning a Class Of Service (COS) to a processor and specifying allocations or limits for that COS for each resource to be allocated. The current COS for a given processor is specified in the PQR_ASSOC MSR, described above. If multiple processors within a QOS domain are assigned the same COS, then the resource allocation associated with that class will be shared among all the processors. At reset, the PQR_ASSOC.COS value is 0.</p> <p data-bbox="632 537 1591 623">For each resource which is managed by the Platform QOS Enforcement feature, a bank of registers is defined which software can program with the allocation limits for each COS. The interpretation of that register depends on the type of resource which is being managed.</p> <p data-bbox="632 651 1255 678">Platform QOS Limits for Cache Allocation Enforcement</p> <p data-bbox="632 695 1608 841">The PQE limits for L3 cache allocation are specified by a bank of MSRs called L3_MASK_n, where “n” is the COS. These registers begin with MSR C90h. There is one register for each COS implemented for that resource. Each of the registers is a bitmask with the MSB at CBM_LEN, which is returned in EAX[4:0] by CPUID Fn0000_0010, EAX=1. (This length is zero-based, so the actual number of QOS bits is EAX[4:0] + 1).</p> <p data-bbox="632 868 1614 1133">Software programs these registers with a bit mask where each “1” represents a portion of the cache which may be used by the corresponding COS. For example, if CBM_LEN for a given implementation is 15, then each “1” which is set in L3_MASK_n represents 1/16 of the cache which may be used by processors running with COS = n. If two or more different Classes of Service have a “1” set in the same bit position in their respective L3_MASK_n register, that represents a portion of the cache which is competitively shared by processors running with those COS values. Some products may implement Cache Allocation Enforcement by allocating some number of ways of the L3 cache for each “1” in the L3_MASK register, but this will not necessarily be true for all implementations and software should not rely on that interpretation.</p> <p data-bbox="632 1161 1640 1377">However, because this is one possible implementation, it is possible that use of PQE for cache allocation will reduce the effective associativity available to processes running using an L3_MASK which does not have all the bits set. The bits which are set in the various L3_MASK_n registers do not have to be contiguous and may overlap in any desired combination. If an L3_MASK_n register is programmed with all 0’s, that COS will be prevented from allocating any lines in the L3 cache. At reset, all L3_MASK_n registers are initialized to all 1’s, allowing all processors to use the entire L3 cache accessible to them.</p>

Claim 1	Identification
	<div>Source: https://web.archive.org/web/20210305161038/https://developer.amd.com/wp-content/resources/56375_1.00.pdf</div> <div><div><div><div><div>63</div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div><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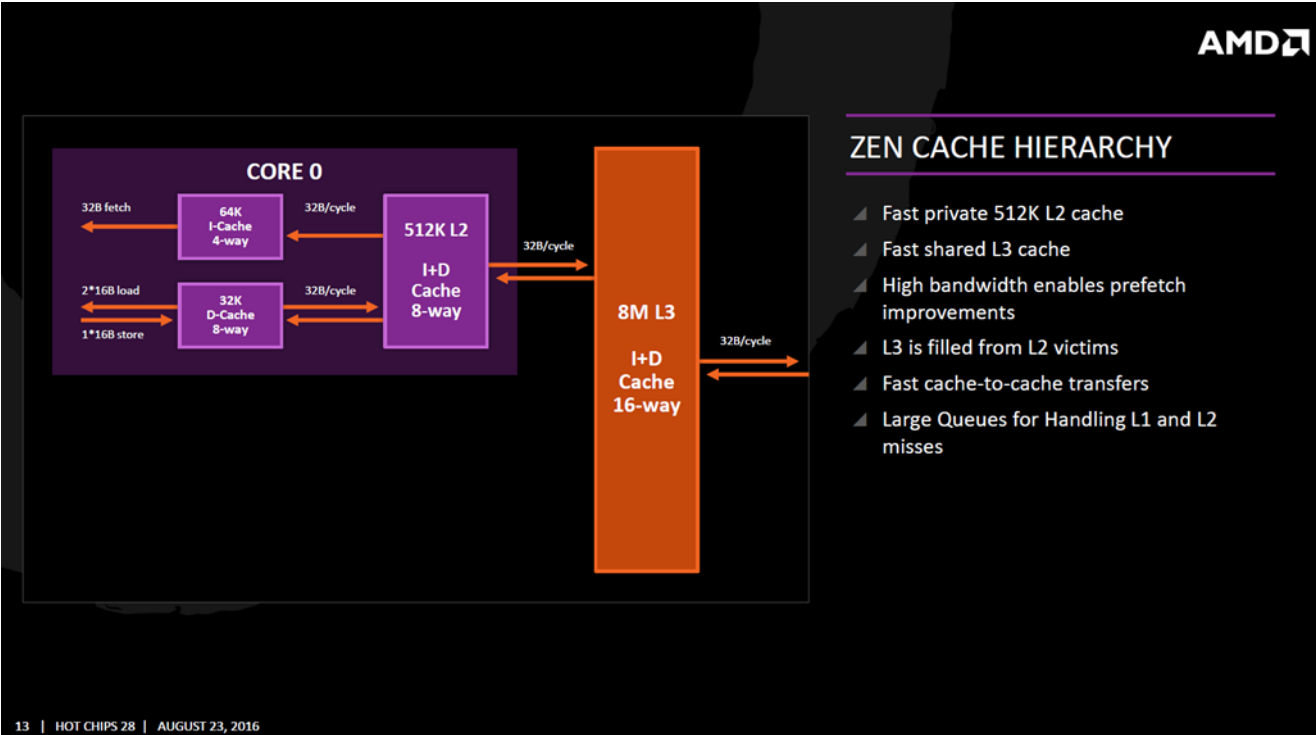
Claim 1	Identification
<p>1[e]. a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, whereby the accessing cache memory controller is allowed to access the allocable cache memory block,</p>	<p>SAP provides a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, whereby the accessing cache memory controller is allowed to access the allocable cache memory block. For example, <i>see</i>:</p> <div data-bbox="583 410 1879 1138"> <p>ZEN CACHE HIERARCHY</p> <ul style="list-style-type: none"> ▲ Fast private 512K L2 cache ▲ Fast shared L3 cache ▲ High bandwidth enables prefetch improvements ▲ L3 is filled from L2 victims ▲ Fast cache-to-cache transfers ▲ Large Queues for Handling L1 and L2 misses </div> <p>13 HOT CHIPS 28 AUGUST 23, 2016</p> <p>Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; <i>see</i> https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.</p>

Claim 1	Identification
	<div data-bbox="577 264 1871 987">  <p>The diagram illustrates the AMD Zen CPU Complex architecture. It shows four cores (CORE 0, CORE 1, CORE 2, CORE 3) arranged in a 2x2 grid. Each core is connected to a local L2 cache (L2M 512K) and a local L3 cache (L3M 1MB). The L3 cache is shared across all four cores. The diagram also shows the L2 cache (L2CTL) and L3 cache (L3CTL) for each core. The AMD logo is in the top right corner.</p> <p>CPU COMPLEX</p> <ul style="list-style-type: none"> ▲ A CPU complex (CCX) is four cores connected to an L3 Cache. ▲ The L3 Cache is 16-way associative, 8MB, mostly exclusive of L2. ▲ The L3 Cache is made of 4 slices, by low-order address interleave. ▲ Every core can access every cache with same average latency <p>14 HOT CHIPS 28 AUGUST 23, 2016</p> </div> <p>Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; see https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.</p>

Claim 1	Identification
	<div data-bbox="581 355 1881 998"> <h2 style="text-align: center;">“ZEN 3” CACHE HIERARCHY (8-CORE)</h2> <ul style="list-style-type: none"> Fast private 512K L2 cache High bandwidth enables prefetch improvements L3 is filled from L2 victims (i.e. mostly exclusive) L2 tags duplicated in L3 for probe filtering and fast cache transfer 64 outstanding misses supported from L2 to L3 per core 192 outstanding misses supported from L3 to memory L3 shared among all 8 cores in the complex </div> <p>Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; see also https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.</p>

Claim 1	Identification
	<p data-bbox="630 282 903 318">QOS Enforcement</p> <p data-bbox="630 334 1606 505">QOS enforcement is accomplished by assigning a Class Of Service (COS) to a processor and specifying allocations or limits for that COS for each resource to be allocated. The current COS for a given processor is specified in the PQR_ASSOC MSR, described above. If multiple processors within a QOS domain are assigned the same COS, then the resource allocation associated with that class will be shared among all the processors. At reset, the PQR_ASSOC.COS value is 0.</p> <p data-bbox="630 534 1577 618">For each resource which is managed by the Platform QOS Enforcement feature, a bank of registers is defined which software can program with the allocation limits for each COS. The interpretation of that register depends on the type of resource which is being managed.</p> <p data-bbox="630 647 1245 673">Platform QOS Limits for Cache Allocation Enforcement</p> <p data-bbox="630 690 1596 833">The PQE limits for L3 cache allocation are specified by a bank of MSRs called L3_MASK_n, where “n” is the COS. These registers begin with MSR C90h. There is one register for each COS implemented for that resource. Each of the registers is a bitmask with the MSB at CBM_LEN, which is returned in EAX[4:0] by CPUID Fn0000_0010, EAX=1. (This length is zero-based, so the actual number of QOS bits is EAX[4:0] + 1).</p> <p data-bbox="630 862 1602 1122">Software programs these registers with a bit mask where each “1” represents a portion of the cache which may be used by the corresponding COS. For example, if CBM_LEN for a given implementation is 15, then each “1” which is set in L3_MASK_n represents 1/16 of the cache which may be used by processors running with COS = n. If two or more different Classes of Service have a “1” set in the same bit position in their respective L3_MASK_n register, that represents a portion of the cache which is competitively shared by processors running with those COS values. Some products may implement Cache Allocation Enforcement by allocating some number of ways of the L3 cache for each “1” in the L3_MASK register, but this will not necessarily be true for all implementations and software should not rely on that interpretation.</p> <p data-bbox="630 1151 1625 1362">However, because this is one possible implementation, it is possible that use of PQE for cache allocation will reduce the effective associativity available to processes running using an L3_MASK which does not have all the bits set. The bits which are set in the various L3_MASK_n registers do not have to be contiguous and may overlap in any desired combination. If an L3_MASK_n register is programmed with all 0’s, that COS will be prevented from allocating any lines in the L3 cache. At reset, all L3_MASK_n registers are initialized to all 1’s, allowing all processors to use the entire L3 cache accessible to them.</p>

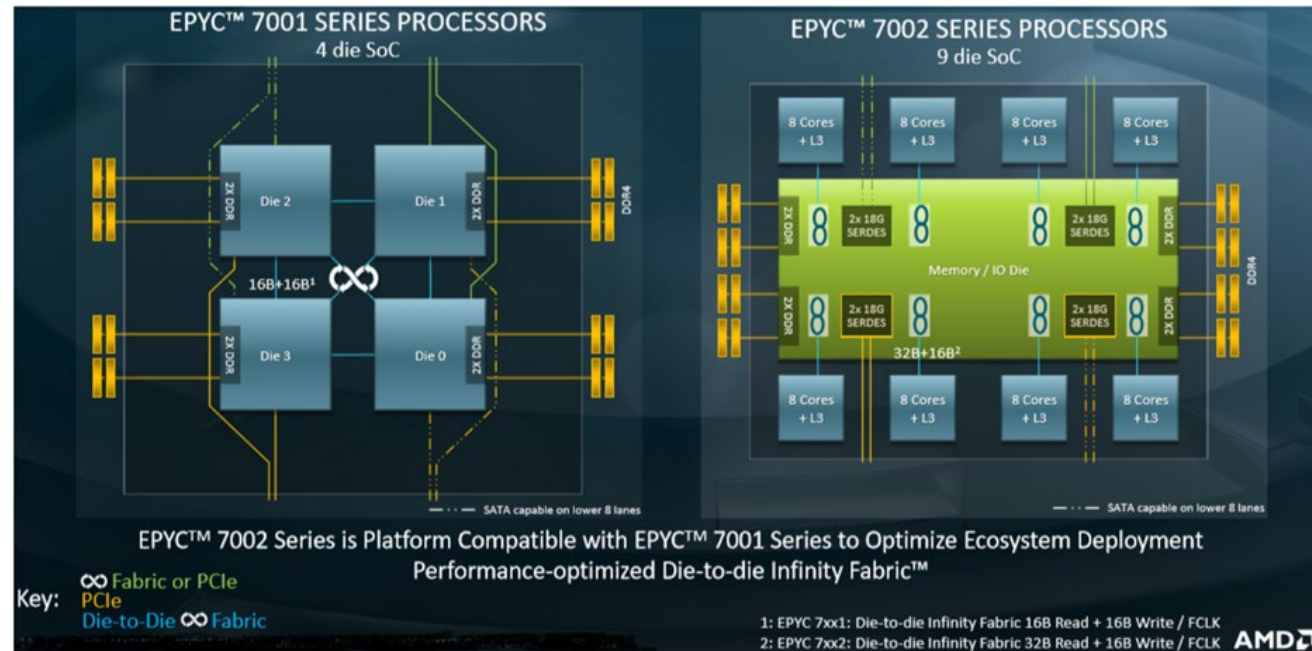
Claim 1	Identification												
	<div>Source: https://web.archive.org/web/20210305161038/https://developer.amd.com/wp-content/resources/56375_1.00.pdf</div> <div><div><div><div>63</div><div>CBM_LEN</div><div>0</div></div><div><div>Reserved, MBZ</div><div>MASK</div></div></div><div>L3_MASK_n, MSR C90h + n</div><div>...</div><div><div><div>63</div><div>CBM_LEN</div><div>0</div></div><div><div>Reserved, MBZ</div><div>MASK</div></div></div><div>L3_MASK_1, MSR C91h</div><div><div><div>63</div><div>CBM_LEN</div><div>0</div></div><div><div>Reserved, MBZ</div><div>MASK</div></div></div><div>L3_MASK_0, MSR C90h</div><table><tr><th>Bits</th><th>Mnemonic</th><th>Description</th><th>R/W</th></tr><tr><td>63:CBM_LEN+1</td><td>Reserved</td><td>Reserved, MBZ</td><td></td></tr><tr><td>CBM_LEN:0</td><td>MASK</td><td>L3 Cache PQE Allocation Mask</td><td>R/W</td></tr></table><div>L3_MASK_<COS> MSR Registers</div></div> <div>Source: https://web.archive.org/web/20210305161038/https://developer.amd.com/wp-content/resources/56375_1.00.pdf</div>	Bits	Mnemonic	Description	R/W	63:CBM_LEN+1	Reserved	Reserved, MBZ		CBM_LEN:0	MASK	L3 Cache PQE Allocation Mask	R/W
Bits	Mnemonic	Description	R/W										
63:CBM_LEN+1	Reserved	Reserved, MBZ											
CBM_LEN:0	MASK	L3 Cache PQE Allocation Mask	R/W										

Claim 1	Identification
<p>1[f]. wherein the cache memory blocks are usable by the cache controllers to store data and instructions fetched from a random-access memory.</p>	<p>SAP provides the resource allocation controller wherein the cache memory blocks are usable by the cache controllers to store data and instructions fetched from a random-access memory. For example, <i>see</i>:</p>  <p>ZEN CACHE HIERARCHY</p> <ul style="list-style-type: none"> ▲ Fast private 512K L2 cache ▲ Fast shared L3 cache ▲ High bandwidth enables prefetch improvements ▲ L3 is filled from L2 victims ▲ Fast cache-to-cache transfers ▲ Large Queues for Handling L1 and L2 misses <p>13 HOT CHIPS 28 AUGUST 23, 2016</p> <p>Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; <i>see</i> https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.</p>

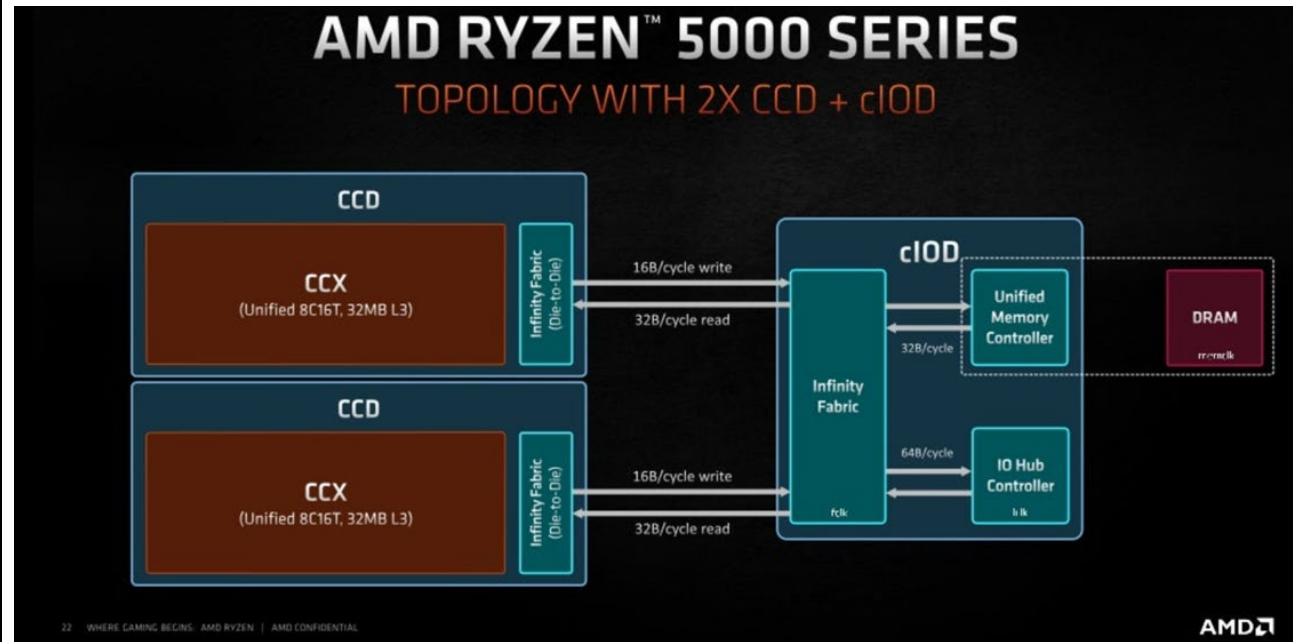
Claim 1	Identification
	<div data-bbox="583 261 1892 959"> <h2 style="text-align: center;">“ZEN 3” CACHE HIERARCHY (8-CORE)</h2> <ul style="list-style-type: none"> Fast private 512K L2 cache High bandwidth enables prefetch improvements L3 is filled from L2 victims (i.e. mostly exclusive) L2 tags duplicated in L3 for probe filtering and fast cache transfer 64 outstanding misses supported from L2 to L3 per core 192 outstanding misses supported from L3 to memory L3 shared among all 8 cores in the complex <p style="text-align: center;">20 WHERE GAMING BEGINS. AMD RYZEN AMD CONFIDENTIAL</p> <p style="text-align: right;">AMD</p> </div> <p>Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; see also https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.</p>

Claim 1

Identification



Source: <https://www.nextplatform.com/2019/08/15/a-deep-dive-into-amds-rome-epyc-architecture/>

Claim 1**Identification**

Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; see also <https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3>.